

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	85	(DUT or (device adj under adj test\$3)) with asynchron\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 18:03
L5	23	(DUT or (device adj under adj test\$3)) with asynchron\$5 with clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 18:03
L8	2	"20050081113".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:20
L9	14035	((device or unit) adj under adj test)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L10	1902	stimulus adj signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L11	321	L9 and L10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L12	466	synchroniz\$5 with (DUT or (device adj under adj test))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L13	0	synchroniz\$5 with (DUT or (device adj under adj test)) with buffer with wirte with read	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28

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L14	10	synchroniz\$5 with (DUT or (device adj under adj test)) with buffer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L15	130	synchroniz\$5 with (DUT or (device adj under adj test)) and buffer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L16	61	synchroniz\$5 with (DUT or (device adj under adj test)) and buffer and write and read	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L17	1921	375/224	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L18	212	synchronization with (DUT or (device adj under adj test))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L19	3	L17 and L18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L20	3	L12 and L17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L21	8	synchronization with (DUT or (device adj under adj test)) and (clock with domain)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28

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L22	239	"26010"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L23	7	"97/26010"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L24	2	"6161160".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L25	2	"5381420".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L26	42	("4430735" "4584683").PN. OR ("4893072").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/05/03 20:28
L27	15	test with pcm with modem	US-PGPUB; USPAT; USOCR	OR	ON	2006/05/03 20:28
L28	146	(synchroniz\$5 with clock) with (DUT or (device adj under adj test))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L29	0	("2002/0141525").URPN.	USPAT	OR	ON	2006/05/03 20:28
L30	15	("4918652" "5081601" "5363319" "5603015" "5678028" "5732247" "5768567" "5790829" "5848236" "5905883" "5987243" "6028996" "6099579" "6115823" "6233540").PN. OR ("6879948"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/05/03 20:28
L31	1	"4534030".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/05/03 20:28

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L32	2	"5499248".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28
L33	2	"5453995".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/03 20:28

Application
Number

SEARCH

IDS Flag Clearance for Application 10032513



Content	Mailroom Date	Entry Number	IDS Review	Reviewer
M844	10-26-2001	9	<input checked="" type="checkbox"/>	05-01-2002 13:26:07 dsavoy

UPDATE



Day : Wednesday
Date: 5/3/2006
Time: 13:02:30

Inventor Information for 10/032513

Inventor Name	City	State/Country
BEHRENS, KLAUS-PETER	GAERTRINGEN	GERMANY
ROTTACKER, MARKUS	STUGGART	GERMANY
MOHR, JOERG-WALTER	EUTINGEN	GERMANY

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Day : Wednesday
Date: 5/3/2006
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Inventor Name Search Result

Your Search was:

Last Name = BEHRENS

First Name = KLAUS-PETER

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07958224	Not Issued	166	10/08/1992	APPARATUS FOR GENERATING TEST SIGNALS	BEHRENS, KLAUS-PETER
08189200	5499248	150	01/31/1994	TEST VECTOR GENERATOR COMPRISING A DECOMPRESSION CONTROL UNIT AND A CONDITIONAL VECTOR PROCESSING UNIT AND METHOD FOR GENERATING A TEST VECTOR	BEHRENS, KLAUS-PETER
08306723	5453995	150	09/15/1994	APPARATUS FOR GENERATING TEST SIGNALS	BEHRENS, KLAUS-PETER
10032513	Not Issued	71	10/26/2001	Data flow synchronization	BEHRENS, KLAUS-PETER
10816646	Not Issued	41	04/02/2004	Parameterized signal conditioning	BEHRENS, KLAUS-PETER
11234447	Not Issued	25	09/23/2005	Source synchronous sampling	BEHRENS, KLAUS-PETER

Inventor Search Completed: No Records to Display.

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Last Name	First Name	
<input type="text" value="BEHRENS"/>	<input type="text" value="KLAUS-PETER"/>	<input type="button" value="Search"/>

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Inventor Name Search Result

Your Search was:

Last Name = ROTTACKER

First Name = MARKUS

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10032513	Not Issued	71	10/26/2001	Data flow synchronization	ROTTACKER, MARKUS
10816646	Not Issued	41	04/02/2004	Parameterized signal conditioning	ROTTACKER, MARKUS
11117968	Not Issued	30	04/29/2005	Pin coupler for an integrated circuit tester	ROTTACKER, MARKUS
11234447	Not Issued	25	09/23/2005	Source synchronous sampling	ROTTACKER, MARKUS

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = MOHR

First Name = JOERG-WALTER

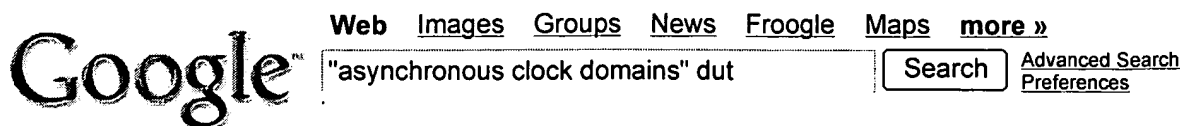
Application#	Patent#	Status	Date Filed	Title	Inventor Name
10032513	Not Issued	71	10/26/2001	Data flow synchronization	MOHR, JOERG-WALTER
11353662	Not Issued	30	02/14/2006	Testing a device under test by sampling its clock and data signal	MOHR, JOERG-WALTER

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Search Another: Inventor	Last Name	First Name	<input type="button" value="Search"/>
	MOHR	JOERG-WALTER	

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Method and apparatus for analyzing digital circuits patent invention

... more **asynchronous clock domains**, wherein clock domain crossing signals are temporarily stored and supplied to a second **DUT** in a time-delayed manner; and ... www.freshpatents.com/Method-and-apparatus-for-analyzing-digital-circuits-dt20050414ptan20050081113.php

Method and apparatus for analyzing digital circuits patent invention

... of a digital circuit design including two or more **asynchronous clock domains**, ... The temporal evolution, that is, the electrical behavior of a **DUT**, ... www.freshpatents.com/Method-and-apparatus-for-analyzing-digital-circuits-dt20050414ptan20050081113.php?ty...

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... report redundant bits of a multi-bit signal crossing **asynchronous clock domains** ... of a create_assign is used In both a checker directive and The **DUT** ... testcompany.com/until-nov2004/2199.html

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DUT. Grounding connection ... synchronisation between these two **asynchronous clock domains**. Figure 29: TS-FO Interface VHDL Code Structure. LINKCNTL ... atlas.web.cern.ch/Atlas/project/cern/ep-atr/download/pubdoc/thesis/haas_thesis.pdf

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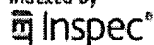
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